# WISHBONE Compatibility Datasheet

The rf68000 core may be directly interfaced to a WISHBONE compatible bus.

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| WISHBONE Datasheet  WISHBONE SoC Architecture Specification, Revision B.3 | | |
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| Description: | Specifications: | |
| General Description: | Central processing unit (CPU core), 68000 compatible | |
| Supported Cycles: | MASTER, READ / WRITE  MASTER, READ-MODIFY-WRITE  MASTER, BLOCK READ / WRITE | |
| Data port, size:  Data port, granularity:  Data port, maximum operand size:  Data transfer ordering:  Data transfer sequencing | 32 bit  8 bit  32 bit  Big Endian (may be configured for little-endian)  any (undefined) | |
| Clock frequency constraints: | none | |
| Supported signal list and cross reference to equivalent WISHBONE signals | Signal Name:  ack\_i  adr\_o(31:0)  clk\_i  dat\_i(31:0)  dat\_o(31:0)  cyc\_o  stb\_o  wr\_o  sel\_o(3:0) | WISHBONE Equiv.  ACK\_I  ADR\_O()  CLK\_I  DAT\_I()  DAT\_O()  CYC\_O  STB\_O  WE\_O  SEL\_O |
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| Special Requirements: |  | |